

Rail-to-rail CMOS dual operational amplifier

Features

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7V to 16V
- Extremely low input bias current: 1pA typ.
- Low input offset voltage: 2mV max.
- Specified for 600 Ω and 100 Ω loads
- Low supply current: 200 μ A/ampl (V_{CC} = 3V)
- Latch-up immunity
- ESD tolerance: 3kV
- Spice macromodel included in this specification

Description

The TS912 is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}⁺ and V_{CC}⁻.

The output reaches:

- V_{CC}⁻ +30mV, V_{CC}⁺ -40mV, with R_L = 10k Ω
- V_{CC}⁻ +300mV, V_{CC}⁺ -400mV, with R_L = 600 Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and supply current of only 200 μ A/amp (V_{CC} = 3V).

Source and sink output current capability is typically 40mA (at V_{CC} = 3V), fixed by an internal limitation circuit.

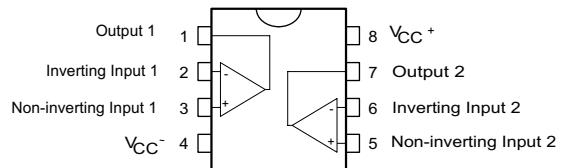


N
DIP-8
(Plastic package)



D
SO-8
(Plastic micropackage)

Pin connections (top view)



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	18	V
V_{id}	Differential input voltage (2)	± 18	V
V_i	Input voltage (3)	-0.3 to 18	V
I_{in}	Current on inputs	± 50	mA
I_o	Current on outputs	± 130	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (4) DIP8 SO-8	85 125	°C/W
R_{thjc}	Thermal resistance junction to case (4) DIP8 SO-8	41 40	°C/W
ESD	HBM: human body model(5)	3	kV
	MM: machine model ⁽⁶⁾	200	V
	CDM: charged device model ⁽⁷⁾	1500	V

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed $V_{CC} + 0.3V$.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These values are typical.
5. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	$V_{CC} - 0.2$ to $V_{CC} + 0.2$	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C

3 Electrical characteristics

Table 3. $V_{CC^+} = 3V$, $V_{CC^-} = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, $A_{VCL} = 1$, no load) $T_{min} \leq T_{amb} \leq T_{max}$		200	300 400	μA
CMR	Common mode rejection ratio $V_{ic} = 0$ to $3V$, $V_o = 1.5V$		70		dB
SVR	Supply voltage rejection ratio ($V_{CC^+} = 2.7$ to $3.3V$, $V_o = V_{CC}/2$)	50	80		dB
A_{vd}	Large signal voltage gain ($R_L = 10k\Omega$, $V_o = 1.2V$ to $1.8V$) $T_{min} \leq T_{amb} \leq T_{max}$	3 2	10		V/mV
V_{OH}	High level output voltage ($V_{id} = 1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	2.95 2.9 2.3 2.6 2	2.96 2.6 2		V
V_{OL}	Low level output voltage ($V_{id} = -1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		30 300 900	50 70 400 100 600	mV
I_o	Output short-circuit current ($V_{id} = \pm 1V$) Source ($V_o = V_{CC^-}$) Sink ($V_o = V_{CC^+}$)	20 20	40 40		mA
GBP	Gain bandwidth product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)		0.8		MHz

Table 3. $V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR ⁺	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to $1.7V$)		0.4		V/ μ s
SR ⁻	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to $1.7V$)		0.3		V/ μ s
ϕm	Phase margin		30		Degrees
en	Equivalent input noise voltage ($R_s = 100\Omega$, $f = 1kHz$)		30		nV/ \sqrt{Hz}

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, $A_{VCL} = 1$, no load) $T_{min} \leq T_{amb} \leq T_{max}$		230	350 450	μA
CMR	Common mode rejection ratio $V_{ic} = 1.5$ to $3.5V$, $V_o = 2.5V$	60	85		dB
SVR	Supply voltage rejection ratio ($V_{CC}^+ = 3$ to $5V$, $V_o = V_{CC}/2$)	55	80		dB
A_{vd}	Large signal voltage gain ($R_L = 10k\Omega$ $V_o = 1.5V$ to $3.5V$) $T_{min} \leq T_{amb} \leq T_{max}$	10 7	40		V/mV
V_{OH}	High level output voltage ($V_{id} = 1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	4.95 4.9 4.25 4.8 4.1	4.95 4.55 3.7		V
V_{OL}	Low level output voltage ($V_{id} = -1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		40 350 1400	50 100 500 150 750	mV
I_o	Output short-circuit current ($V_{id} = \pm 1V$) Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)	45 45	65 65		mA
GBP	Gain bandwidth product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)		1		MHz
SR ⁺	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1V$ to $4V$)		0.8		$V/\mu s$
SR ⁻	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1V$ to $4V$)		0.6		$V/\mu s$

Table 4. $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
en	Equivalent input noise voltage ($R_s = 100\Omega$, $f = 1kHz$)		30		nV/ \sqrt{Hz}
V_{O1}/V_{O2}	Channel separation ($f = 1kHz$)		120		dB
ϕ_m	Phase margin		30		Degrees

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. $V_{CC^+} = 10V$, $V_{CC^-} = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, $A_{VCL} = 1$, no load) $T_{min} \leq T_{amb} \leq T_{max}$		400	600 700	μA
CMR	Common mode rejection ratio $V_{ic} = 3$ to $7V$, $V_o = 5V$ $V_{ic} = 0$ to $10V$, $V_o = 5V$	60 50	90 75		dB
SVR	Supply voltage rejection ratio ($V_{CC^+} = 5$ to $10V$, $V_o = V_{CC}/2$)	60	90		dB
A_{vd}	Large signal voltage gain ($R_L = 10k\Omega$, $V_o = 2.5V$ to $7.5V$) $T_{min} \leq T_{amb} \leq T_{max}$	15 10	50		V/mV
V_{OH}	High level output voltage ($V_{id} = 1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	9.95 9.85 9 9.8 8.8	9.95 9.35 7.8		V
V_{OL}	Low level output voltage ($V_{id} = -1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		50 650 2300	50 150 800 150 900	mV
I_o	Output short circuit current ($V_{id} = \pm 1V$) Source ($V_o = V_{CC^-}$) Sink ($V_o = V_{CC^+}$)	45 50	65 75		mA
GBP	Gain bandwidth product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)		1.4		MHz

Table 5. $V_{CC}^+ = 10V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR ⁺	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 2.5V$ to $7.5V$)		1.3		V/ μ s
SR ⁻	Slew rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 2.5V$ to $7.5V$)		0.8		V/ μ s
ϕ_m	Phase margin		40		Degrees
en	Equivalent input noise voltage ($R_s = 100\Omega$, $f = 1kHz$)		30		nV/ \sqrt{Hz}
THD	Total harmonic distortion ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_o = 4.75V$ to $5.25V$, $f = 1kHz$)		0.02		%
C_{in}	Input capacitance		1.5		pF

1. Maximum values include unavoidable inaccuracies of the industrial tests.

5.1 DIP-8 package mechanical data

Figure 15. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

The figure contains four technical drawings of the DIP8 package:

- Top View:** Shows the package in a rectangular outline with pins numbered 1 through 8. Dimensions include D (width), E1 (height), and the pin spacing.
- Side View:** Shows the package in perspective with dimensions A, A1, A2, b, b2, c, D, E, E1, and e.
- Front View:** Shows the package from the front with dimensions E, eA, eB, and c.
- Cross-Sectional View:** Shows a vertical cut through the package. It includes a callout labeled "GAUGE PLANE 0.38" pointing to a horizontal line at a height of 0.38 units from the bottom. Other dimensions shown are E, H, and E1.

6 Ordering information

Table 6. Order codes

Part number	Temperature range	Package	Packing	Marking	
TS912IN	-40°C, +125°C	DIP8	Tube	TS912IN	
TS912AIN				TS912AIN	
TS912ID		SO-8	Tube or Tape & reel	912I	
TS912IDT				912AI	
TS912AID				912BI	
TS912AIDT				912IY	
TS912BID				912AIY	
TS912BIDT		SO-8 (Automotive grade level)		912BY	
TS912IYD					
TS912IYDT ⁽¹⁾					
TS912AIYD					
TS912AIYDT ⁽¹⁾					
TS912BIYD					
TS912BIYDT ⁽¹⁾					

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.